IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Bohumil Lojek PATENT APPLICATION

Serial No.: 10/761,876 Group Art Unit: 2812

Filed: January 21, 2004 Examiner:

For: VERTICAL GATE CMOS WITH LITHOGRAPHY-INDEPENDENT

GATE LENGTH

Supplemental Information Disclosure Statement

Hon. Commissioner for Patents Alexandria, VA 22313

Sir:

The following information is submitted in compliance with Applicant's duty of disclosure under 37 CFR § 1.56. A copy of the reference is enclosed.

Other References

- J. M. Hergenrother et al. (Bell Laboratories, Lucent Technologies), Murray Hill, NJ, "The Vertical Replacement-Gate (VRG) MOSFET: A 50-nm Vertical MOSFET with Lithography-Independent Gate Length", IEEE 1999 International Electron Devices Meeting, pp. 3.6.1 3.6.4.
- D. Monroe et al. (Lucent Technologies, Bell Labs Innovations), "Revolutionary Transistor Turns Silicon World on End", April 2000, Lucent Technologies, 3 pages.

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This statement is believed to be filed before the mailing date of a first Office action on the merits. Applicant respectfully requests consideration by the PTO of the submitted information.

CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box

1450, Alexandria, PA 2273-1450
Signed: Schule Cerpuedo

Typed Name: Sally Azevedo

Date: May 13, 2004

Respectfully submitted,

Thomas Schneck Reg. No. 24,518

P.O. Box 2-E San Jose, CA 95109-0005 (408) 297-9733

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